



LinearDimensions
SEMICONDUCTOR

LND34063A

DC-to-DC Converter Control Circuits

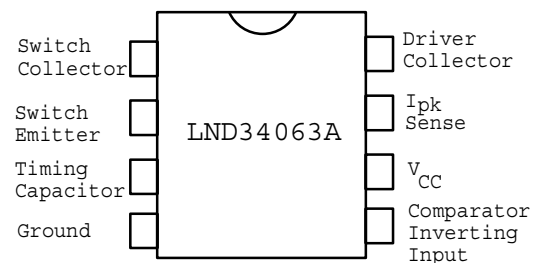
GENERAL DESCRIPTION

The LND34063A is a monolithic control circuit containing the primary functions required for DC-to-DC converters. This device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This device was specifically designed to be incorporated in Step-down and Step-up and Voltage-Inverting applications with a minimum number of external components.

FEATURES

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5A
- Frequency Operation to 100kHz
- Precision 2% Reference

PIN CONNECTIONS

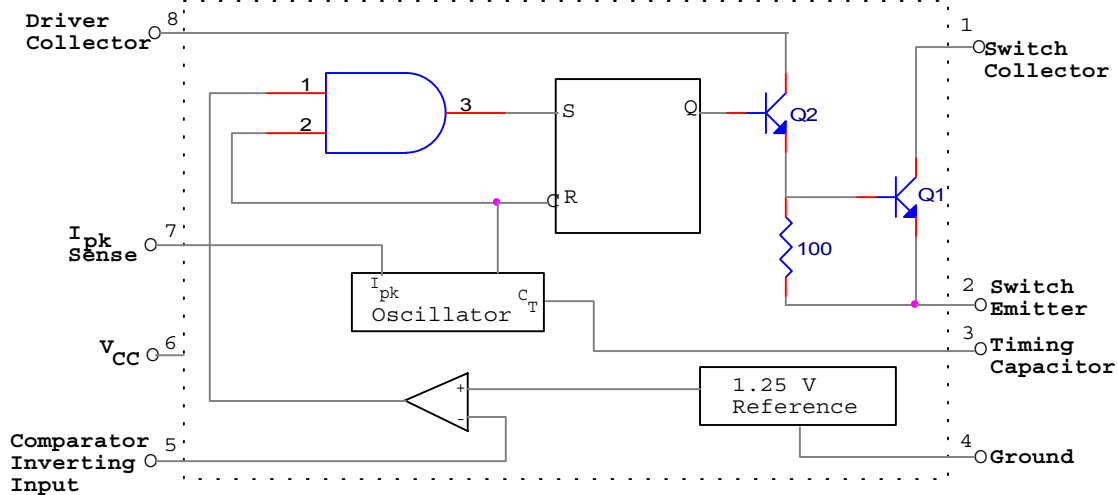




ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	40	Vdc
Comparator Input Voltage Range	V _{IR}	-0.3 to +40	Vdc
Switch Collector Voltage	V _{C(Switch)}	40	Vdc
Switch Emitter Voltage(V _{pin} =40V)	V _{E(switch)}	40	Vdc
Switch Collector to Emitter Voltage	V _{CE(switch)}	40	Vdc
Driver Collector Voltage	V _{C(driver)}	40	Vdc
Driver Collector Current(Note 1)	I _{C(driver)}	100	mA
Switch Current	I _{sw}	1.5	A
Operating Junction Temperature	T _J	+150	°C
Operating Ambient Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	-65 to +150	°C

SCHEMATIC DIAGRAM





ELECTRICAL CHARACTERISTICS

V_{cc}=5.0V, T_A=T_{low} to T_{high}, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
Oscillator					
Frequency (V _{pin5} =0V, C _T =1.0nF, T _A =25°C)	f _{osc}	24	33	42	kHz
Charge Current (V _{cc} =5.0V to 40V, T _A =25°C)	I _{chg}	24	35	42	μA
Discharge Current (V _{cc} =5.0V to 40V, T _A =25°C)	I _{dischg}	140	220	260	μA
Discharge to charge Current ratio (Pin 7 to V _{cc} , T _A =25°C)	I _{dischg} /I _{chg}	5.2	6.5	7.5	-
Current Limit Sense Voltage (I _{chg} =I _{dischg} , T=25°C)	V _{ipk(sense)}	250	300	350	mV
Output Switch(Note 2)					
Saturation Voltage Darlington Connection (I _{sw} =1.0 A, Pins 1,8 connected)	V _{ce(sat)}	-	1.0	1.3	V
Saturation Voltage, Darlington Connection (I _{sw} =1.0A, R _{pin8} =82Ω to V _{cc} , forcedβ=20)	V _{ce(sat)}	-	0.45	0.7	V
DC Current Gain (I _{sw} =1.0A, V _{ce} =5.0V T _A = 25° C)	h _{FE}	50	75	-	-
Collector Off-State Current (V _{ce} =40V)	I _{c(off)}	-	40	100	μA
Comparator					
Threshold Voltage (T _A =25°C) (T _A =T _{low} to T _{high})	V _{th}	1.225 1.21	1.25 -	1.275 1.29	V
Threshold Voltage Line Regulation (V _{cc} =3.0V to 40V)	Reg _{line}	-	1.4	5.0	mV
Input Bias Current (V _{in} =0V)	I _{IB}	-	-20	-400	nA
Total Device					
Supply Current (V _{cc} =5.0V to 40V, C _t =1.0nF, Pin 7=V _{cc} , V _{pin 5} >V _{th} , Pin 2=Gnd, remaining pins open)	I _{cc}	-	-	4.0	mA

Notes:

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.



SOME TYPICAL APPLICATIONS

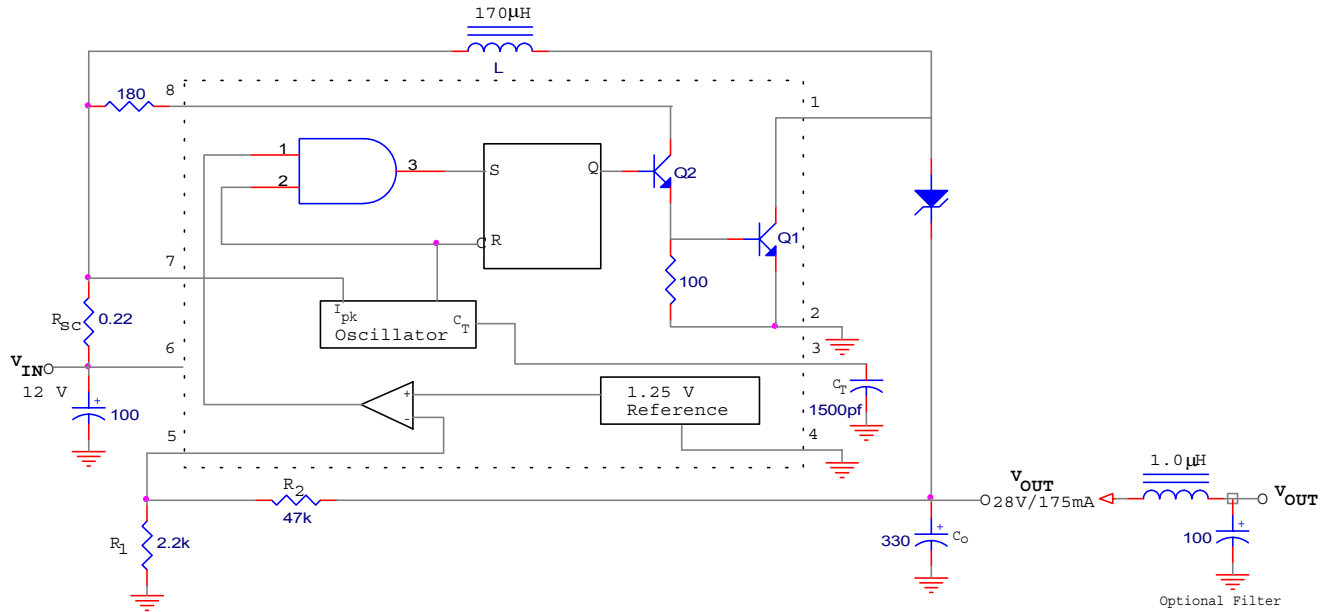


Fig 1 : STEP UP CONVERTER

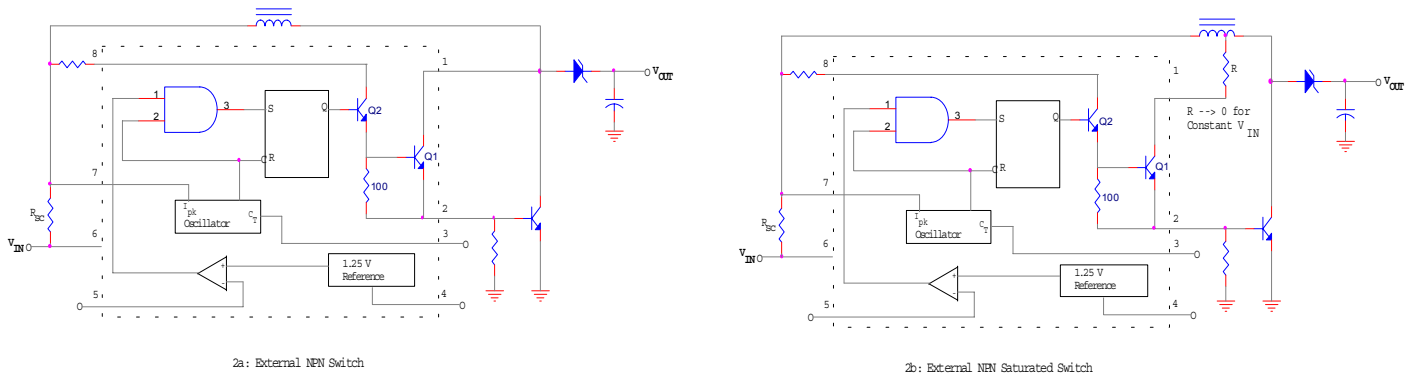


Fig 2 : External Boost Connections
for I_c Peak Greater than 1.5A

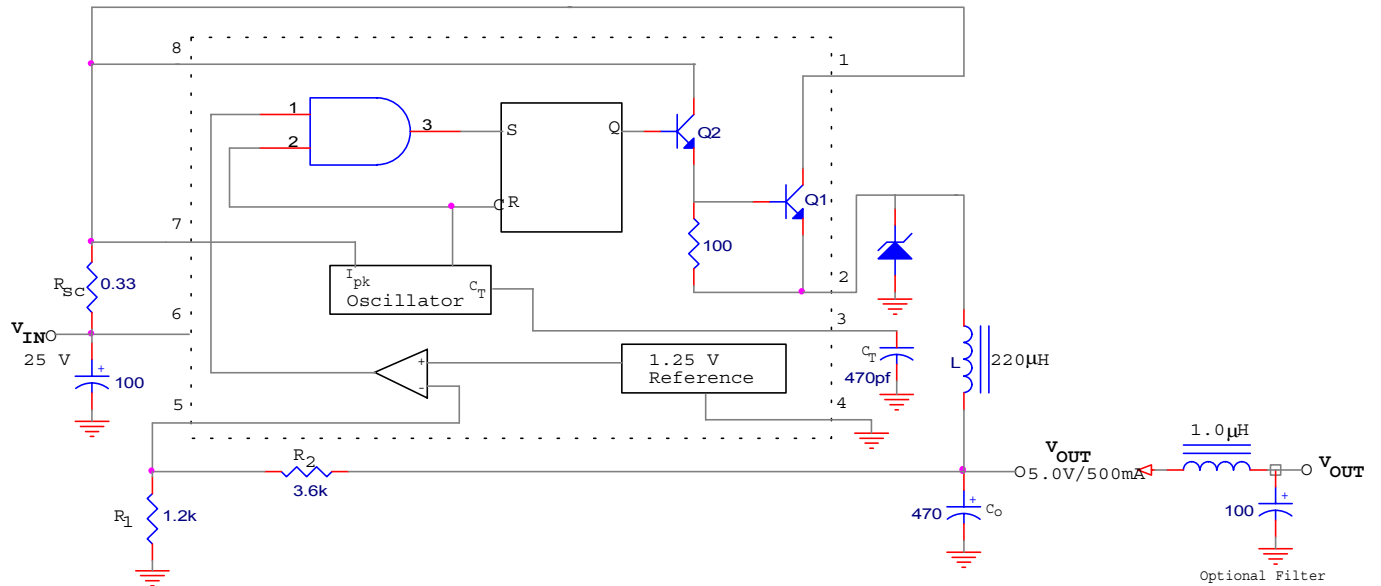


Fig 3 : STEP DOWN CONVERTER

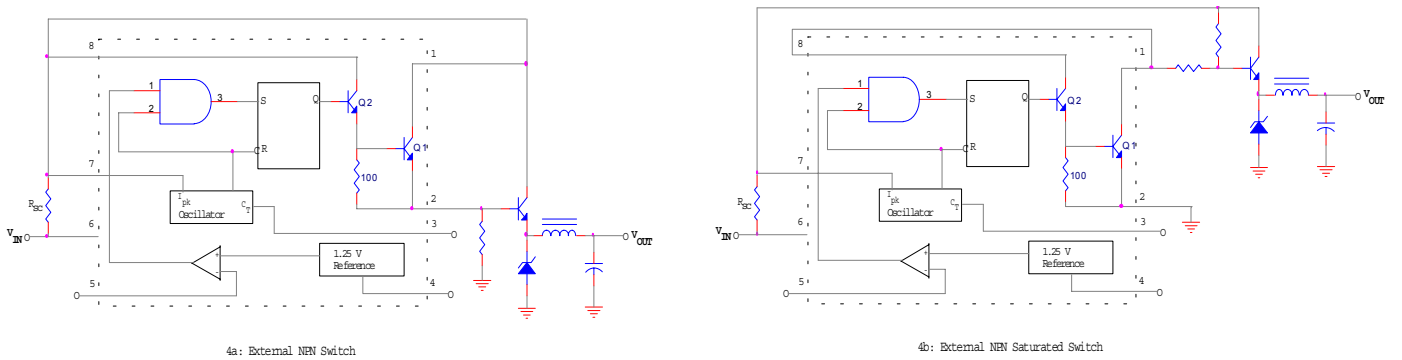


Fig4 : External Boost Connections
for I_c Peak Greater than 1.5A

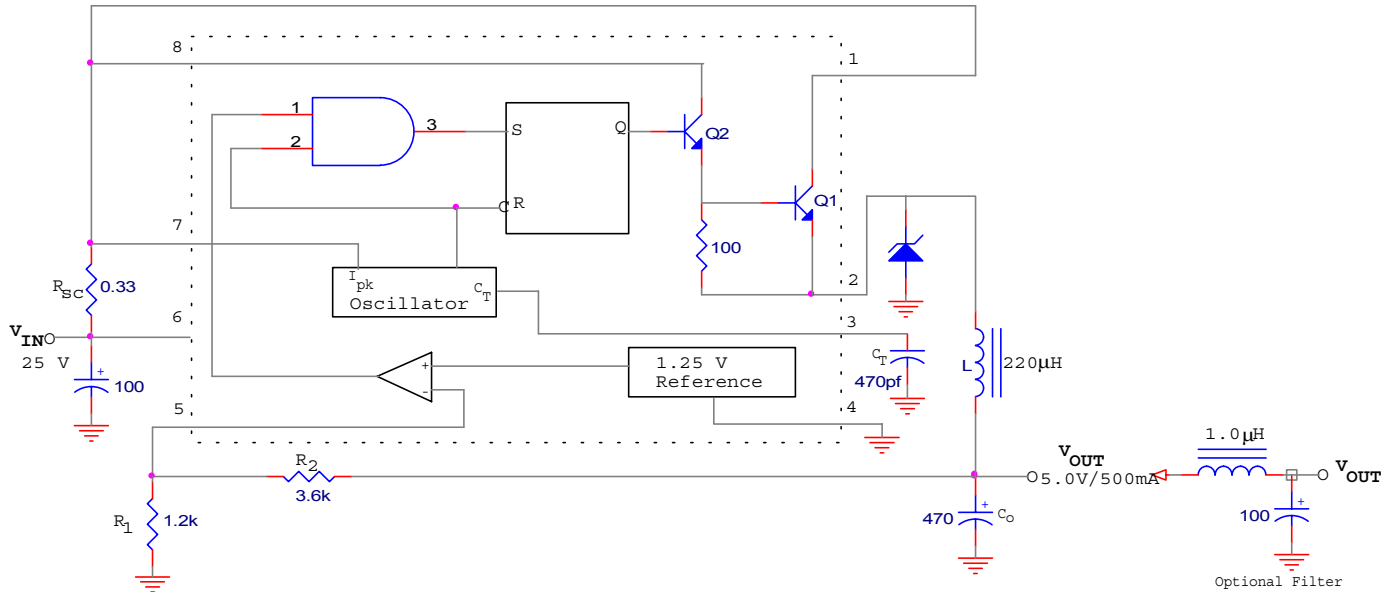
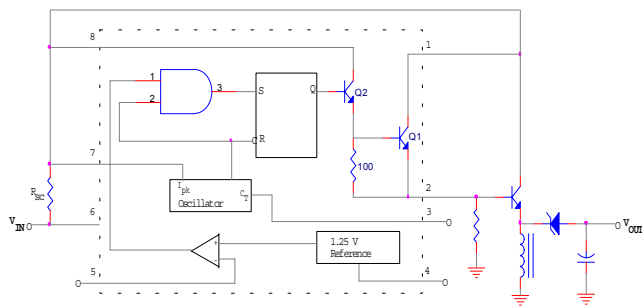
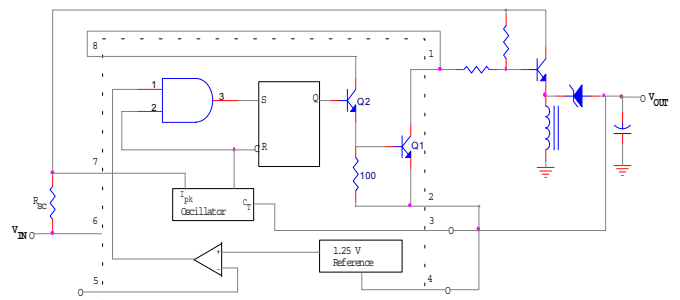


Fig 5 : VOLTAGE INVERTING CONVERTER



6a: External NEN Switch



6b: External NEN Saturated Switch

Fig6 : External Boost Connections
for I_c Peak Greater than 1.5A



Figure 7: Design Formula Table

Calculation	Step-Up	Step-down	Voltage-Inverting
t_{ON}/t_{OFF}	$(V_{out}+V_F-V_{IN(min)}) / (V_{IN(min)}-V_{sat})$	$(V_{out}+V_F) / (V_{in(min)}-V_{sat}-V_{out})$	$(V_{out}+V_F) / (V_{in}-V_{sat})$
$(t_{ON}/t_{OFF})_{max}$	$1/ f_{MIN}$	$1/ f_{MIN}$	$1/ f_{MIN}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{PK(switch)}$	$2 I_{out (max)}(t_{on}/t_{off} + 1)$	$2 I_{out(max)}$	$2 I_{out (max)}(t_{on}/t_{off} + 1)$
R_{SC}	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$	$0.3 / I_{pk(switch)}$
$L_{(min)}$	$(V_{in(min)}-V_{sat})/(I_{pk(switch)})=t_{out(max)}$	$(V_{in(min)}-V_{sat}-V_{out}) / (I_{pk(switch)}) = t_{out(max)}$	$(V_{in(min)}-V_{sat}) / (I_{pk(switch)}) = t_{out(max)}$
C_O	$9(I_{out}t_{on}) / (V_{ripple(pp)})$	$I_{pk(switch)} (t_{on} + t_{off}) / 8V_{ripple(pp)}$	$9(I_{out}t_{on}) / (V_{ripple(pp)})$

Terms and Definitions

V_{sat} -Saturation voltage of the output switch
 V_F —Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{IN} -Nominal input voltage
 V_{out} -Desired output voltage, $|V_{out}|=1.25 (1 +R_2 / R_1)$
 I_{OUT} -Desired output current
 f_{min} -Minimum desired output switching frequency at the selected values of V_{IN} and I_O
 $V_{ripple(p-p)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.